Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] CLAIMS

1.A method for implementing a self-timed, read to write operation in a memory storage device, the method comprising:

capturing a read address during a first half of a current clock cycle;

commencing a read operation so as to read data corresponding to said captured read address onto a pair of bit lines;

commencing a write operation for said current clock cycle so as to cause write data to appear on said pair of bit lines as soon as said read data from said captured read address is amplified by a sense amplifier, wherein said write operation uses a previous write address captured during a preceding clock cycle; and

capturing a current write address during a second half of said current clock cycle, said current write address to be used for a write operation implemented during a subsequent clock cycle;

wherein said commencing a write operation for said current clock cycle is timed independent of said current write address captured during said second half of said

current clock cycle.

[c2] 2.The method of claim 1, further comprising:
generating an internal read clock signal from a main clock signal;
generating a first internal write clock signal from said main clock signal, said first internal write clock signal used for said capturing a current write address; and
generating a second internal write clock signal from said main clock signal, said second internal write clock signal used for commencing a write operation for said current clock cycle;
wherein said second internal write clock signal is also a delayed version of said internal read clock signal.

[c3] 3.The method of claim 2, further comprising implementing sense amplifier interlock logic to enable said write operation to cause write data to appear on said pair of bit lines as soon as said read data from said captured read address is amplified by said sense amplifier.

[c4] 4.The method of claim 3, wherein said sense amplifier interlock logic utilizes a mimic word line to simulate a signal delay propagated through an actual word line and bit line during said read operation.

[c5] 5.The method of claim 4, wherein said sense amplifier

interlock logic is used to control a pair of read bit switches configured to selectively couple said bit lines to said sense amplifier, and said sense amplifier interlock logic is further used to control a pair of write bit switches configured to selectively couple said bit lines to a write driver.

[c6] 6.The method of claim 5, wherein said sense amplifier interlock logic is used to reset a subarray of the memory storage device and disable a read-operation word line prior to the start of said write operation.

[c7] 7.The method of claim 6, wherein said sense amplifier interlock logic is used to reset said subarray of the memory storage device, disable a write-operation word line, and initiate a bit line precharge operation using a write margin mimic delay circuit configured to simulate the timing margin of said write operation.

[c8] 8.The method of claim 6, wherein said sense amplifier interlock logic is used to control the operation of said write driver.

[c9] 9.A method for implementing a self-timed, read to write protocol for a Quad Data Rate (QDR) Static Random Access Memory (SRAM) device, the method comprising: capturing a read address during a first half of a current

clock cycle;

commencing a read operation so as to read data corresponding to said captured read address onto a pair of bit lines;

commencing a write operation for said current clock cycle so as to cause write data to appear on said pair of bit lines as soon as said read data from said captured read address is amplified by a sense amplifier, wherein said write operation uses a previous write address captured during a preceding clock cycle; and

capturing, in a write address buffer, a current write address during a second half of said current clock cycle, said current write address to be used for a write operation implemented during a subsequent clock cycle;

wherein said commencing a write operation for said current clock cycle is timed independent of said current write address captured during said second half of said current clock cycle.

[c10] 10.The method of claim 9, further comprising:

generating an internal read clock signal from a main clock signal;

generating a first internal write clock signal from said main clock signal, said first internal write clock signal used for said capturing a current write address; and

generating a second internal write clock signal from said

main clock signal, said second internal write clock signal used for commencing a write operation for said current clock cycle;

wherein said second internal write clock signal is also a delayed version of said internal read clock signal.

[c11] 11.The method of claim 10, further comprising implementing sense amplifier interlock logic to enable said write operation to cause write data to appear on said pair of bit lines as soon as said read data from said captured read address is amplified by said sense amplifier.

[c12] 12.The method of claim 11, wherein said sense amplifier interlock logic utilizes a mimic word line to simulate a signal delay propagated through an actual word line and bit line during said read operation.

[c13] 13.The method of claim 12, wherein said sense amplifier interlock logic is used to control a pair of read bit switches configured to selectively couple said bit lines to said sense amplifier, and said sense amplifier interlock logic is further used to control a pair of write bit switches configured to selectively couple said bit lines to a write driver.

[c14] 14.The method of claim 13, wherein said sense amplifier interlock logic is used to reset a subarray of the memory

storage device and disable a read-operation word line prior to the start of said write operation.

[c15] 15.The method of claim 14, wherein said sense amplifier interlock logic is used to reset said subarray of the memory storage device, disable a write-operation word line, and initiate a bit line precharge operation using a write margin mimic delay circuit configured to simulate the timing margin of said write operation.

[c16] 16.The method of claim 14, wherein said sense amplifier interlock logic is used to control the operation of said write driver.

[c17] 17.The method of claim 9, further comprising:
comparing said current write address in said write address buffer with said current read address; and
upon determining a match between said current read address and said current write address, fetching said read data from a write data buffer.

[c18] 18.A semiconductor memory storage device, comprising:
circuitry configured to capture a read address during a first half of a current clock cycle;
circuitry configured to commence a read operation so as to read data corresponding to said captured read address onto a pair of bit lines;

circuitry configured to commence a write operation for said current clock cycle so as to cause write data to appear on said pair of bit lines as soon as said read data from said captured read address is amplified by a sense amplifier, wherein said write operation uses a previous write address captured during a preceding clock cycle; and

circuitry configured to capture a current write address during a second half of said current clock cycle, said current write address to be used for a write operation implemented during a subsequent clock cycle;

wherein said write operation for said current clock cycle is timed independent of said current write address captured during said second half of said current clock cycle.

[c19] 19.The memory storage device of claim 18, further comprising:

circuitry configured to generate an internal read clock signal from a main clock signal;

circuitry configured to generate a first internal write clock signal from said main clock signal, said first internal write clock signal used for said capturing a current write address; and

circuitry configured to generate a second internal write clock signal from said main clock signal, said second internal write clock signal used for commencing a write

operation for said current clock cycle;
wherein said second internal write clock signal is also a delayed version of said internal read clock signal.

[c20] 20.The method of claim 19, further comprising sense amplifier interlock logic configured to enable said write operation to cause write data to appear on said pair of bit lines as soon as said read data from said captured read address is amplified by said sense amplifier.

[c21] 21.The memory storage device of claim 20, wherein said sense amplifier interlock logic utilizes a mimic word line to simulate a signal delay propagated through an actual word line and bit line during said read operation.

[c22] 22.The memory storage device of claim 21, wherein said sense amplifier interlock logic is configured to control a pair of read bit switches configured to selectively couple said bit lines to said sense amplifier, said sense amplifier interlock logic further configured to control a pair of write bit switches configured to selectively couple said bit lines to a write driver.

[c23] 23.The method of claim 22, wherein said sense amplifier interlock logic is configured to reset a subarray of the memory storage device and disable a read-operation word line prior to the start of said write operation.

[c24] 24.The memory storage device of claim 23, wherein said sense amplifier interlock logic is configured to reset said subarray of the memory storage device, disable a write-operation word line, and initiate a bit line precharge operation using a write margin mimic delay circuit configured to simulate the timing margin of said write operation.

[c25] 25.The memory storage device of claim 22, wherein said sense amplifier interlock logic is configured to control the operation of said write driver.

[c26] 26.A Quad Data Rate (QDR) Static Random Access Memory (SRAM) device, comprising:
circuitry configured to capture a read address during a first half of a current clock cycle;
circuitry configured to commence a read operation so as to read data corresponding to said captured read address onto a pair of bit lines;
circuitry configured to commence a write operation for said current clock cycle so as to cause write data to appear on said pair of bit lines as soon as said read data from said captured read address is amplified by a sense amplifier, wherein said write operation uses a previous write address captured during a preceding clock cycle; and

circuitry configured to capture, in a write address buffer, a current write address during a second half of said current clock cycle, said current write address to be used for a write operation implemented during a subsequent clock cycle;

wherein said write operation for said current clock cycle is timed independent of said current write address captured during said second half of said current clock cycle.

[c27] 27.The QDR SRAM device of claim 26, further comprising:

circuitry configured to generate an internal read clock signal from a main clock signal;

circuitry configured to generate a first internal write clock signal from said main clock signal, said first internal write clock signal used for said capturing a current write address; and

circuitry configured to generate a second internal write clock signal from said main clock signal, said second internal write clock signal used for commencing a write operation for said current clock cycle;

wherein said second internal write clock signal is also a delayed version of said internal read clock signal.

[c28] 28.The QDR SRAM device of claim 27, further comprising sense amplifier interlock logic configured to enable said write operation to cause write data to appear on said pair

of bit lines as soon as said read data from said captured read address is amplified by said sense amplifier.

[c29] 29.The QDR SRAM device of claim 28, wherein said sense amplifier interlock logic utilizes a mimic word line to simulate a signal delay propagated through an actual word line and bit line during said read operation.

[c30] 30.The QDR SRAM device of claim 29, wherein said sense amplifier interlock logic is configured to control a pair of read bit switches configured to selectively couple said bit lines to said sense amplifier, said sense amplifier interlock logic further configured to control a pair of write bit switches configured to selectively couple said bit lines to a write driver.

[c31] 31.The QDR SRAM device of claim 30, wherein said sense amplifier interlock logic is configured to reset a subarray of the memory storage device and disable a read-operation word line prior to the start of said write operation.

[c32] 32.The QDR SRAM device of claim 31, wherein said sense amplifier interlock logic is configured to reset said subarray of the memory storage device, disable a write-operation word line, and initiate a bit line precharge operation using a write margin mimic delay circuit config-

ured to simulate the timing margin of said write operation.

[c33] 33.The QDR SRAM device of claim 30, wherein said sense amplifier interlock logic is configured to control the operation of said write driver.

[c34] 34.The QDR SRAM device of claim 26, further comprising:

a comparator configured to compare said current write address in said write address buffer with said current read address; and

circuitry configured to fetch said read data from a write data buffer upon determination of a match between said current read address and said current write address.